Random Noise Improvement for Pixel-Parallel Single-Slope ADC

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ABSTRACT

Low random noise (RN) design for pixel-parallel single-slope ADC (SS-ADC) in digital pixel sensor (DPS) is reported. The AC-based RN estimation with respect to the comparator bias current and bandwidth-limiting capacitor in DPS is discussed. RN is composed of thermal noise (TN) and flicker noise (FN), and FN easily becomes the major contributor in DPS. Low RN design comparable to that in digital correlated double sampling (D-CDS) scheme is considered after studying FN characteristics modulated by CDS operation. High gain single-ended comparator is introduced to realize area-efficient DPS. It achieved the low RN of 2.4e-rms in 3.24um pixel by 10-bit in-pixel memory without D-CDS. High dynamic range (DR) was demonstrated using dual quantization operation with 2 conversion gains in single exposure.

I. INTRODUCTION

Correlated double sampling (CDS) is originally applied as RN suppression technique toward floating diffusion (FD) reset noise in CCD [1]. It was improved as D-CDS technique for column-parallel SS-ADC in CMOS image sensor (CIS) combined with analog-CDS (A-CDS) [2]. D-CDS suppresses not only FPN but also RN after A-CDS. It suppresses reset noise of comparator auto-zero (AZ) operation after pixel FD reset noise suppression by A-CDS. Low noise less than 1e-rms is reported by D-CDS [3]. Main contributor for low noise is narrow noise bandwidth (nBW) of comparator in column-parallel configuration and high conversion gain (HCG).

D-CDS is also applicable to pixel-parallel ADC [4,5,6], but their RN is larger than those in column-parallel configuration due to the small digital pixel area. In this report, effectiveness of RN reduction with D-CDS technique is investigated based on the DPS architecture reported in [7]. Low RN design suitable for small pixel is implemented and demonstrated.

II. Random Noise in SS-ADC

Simplified circuit diagram of the pixel-parallel ADC circuit in [7] is shown in Fig. 1. Circuit in Fig. 1 is equivalent to conventional column-parallel SS-ADC configuration. Pixel bias I_{bs}, comparator and memory are included in each column in column-parallel ADC, and their area and bias current restrictions are relaxed compared to pixel-parallel ADC sensors. 4-transistor active pixel output is connected to negative input of differential amplifier through coupling capacitance of C_C. The comparator output is connected to load capacitor C_{bw} and inverter stage. Higher C_{bw} reduces nBW. Low noise characteristics with large C_{bw} is demonstrated [8]. However, the maximum C_{bw} size is restricted by available device and pixel size. As a result, the sizes of C_C and C_{bw} should be carefully considered in pixel-parallel configuration.

D-CDS operation timing diagram is shown in Fig. 2. Pixel reset operation of RST=H to L induces reset noise at FD. It is suppressed by comparator AZ operation through feedback switch in differential amplifier with operation AZ=H to L leaving sampling noise in C_C at T0.

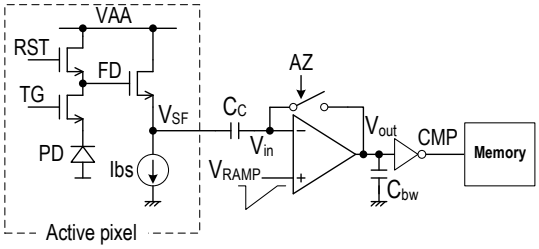

Fig. 1 Pixel-parallel SS-ADC circuit in [7].

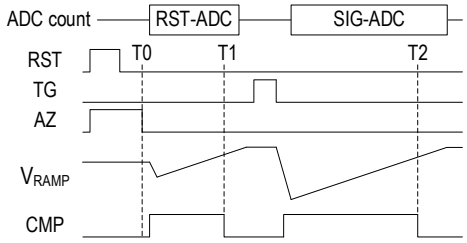

Fig. 2 Operation timing diagram of SS-ADC with D-CDS.

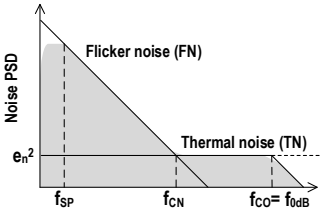

Fig. 3 (a) Noise PSD at T0.

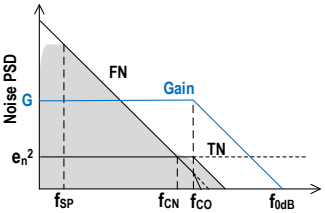

Fig. 3 (b) Noise PSD at T1 and T2

Fig.3 (a) and Fig.3 (b) shows conceptual RN power spectrum density (PSD) at T0 and T2 (T1). PSD in T1 is same as that in T2. Cut-off frequency f_{CO} matches unity gain frequency f_{0dB} at T0 when AZ operation completes, and it becomes lower at T2 when the comparator is open-loop condition with a gain G. D-CDS suppresses RN and FPN at T0, while RN is introduced at T1. In column SS-ADC, D-CDS works effectively because RN at T0 is a few times larger than RN at

T1 with a high f_{CO}. On the other hand, it should be carefully considered in DPS because bias current and area assignment for C_C, C_{bw} and memory are restricted.

III. Random noise estimation

Exact RN should be calculated after noise PSD modulation with sampling frequency f_{SP} in CDS circuit, however it is neglected in this paper since it does not impact the conceptual noise study.

Comparator RN is the main noise contributor in DPS in [7]. RN at V_{out} in Fig. 1 is written as equation (1). The first term inside the bracket is thermal noise (TN), and the second term is flicker noise (FN). Parameters are explained in Table 1.

$$v_{no}{}^2 = G^2 \int \left\{ e_n{}^2 + \frac{f_{CN}}{f} e_n{}^2 \right\} df \quad (1)$$

Assuming a simple differential amplifier as the comparator input stage, noise floor e_n and cut-off frequency f_{CO} are expressed with equations (2) and (3), respectively.

$$e_n{}^2 = 2\frac{4kT\gamma}{g_{mi}}\left(1 + \frac{g_{mo}}{g_{mi}}\right) \quad (2)$$

$$f_{CO} = \frac{g_{mi}}{2\pi G C_{bw}} \quad (3)$$

Input referred RN, v_{ni} is formulated as equation (4) by applying equations (2) and (3) to equation (1). In this equation, nBW coefficient of $\pi/2$ [9] is included in TN integral calculation, but it is omitted in FN calculation for less impact. FN noise term also uses constant b for integral noise value under f_{SP} in CDS operation, which is around 2.5 by numerical integral calculation.

$$v_{ni}{}^2 = \frac{v_{no}{}^2}{G^2} = \frac{2\gamma kT}{GC_{bw}}\left(1 + \frac{g_{mo}}{g_{mi}}\right) + e_n{}^2 f_{CN}\left(ln\frac{f_{CO}}{f_{SP}} + b\right) \quad (4)$$

Equations (3) and (4) are assuming RN at T1 and T2 in Fig. 2 of open-loop condition. GC_{bw} in equations (3) and (4) are replaced with $C_C + C_{bw}$ at T0 because ON status of AZ switch makes closed-loop gain to be 1 and adding parallel load of C_C. CDS sampling frequency f_{SP} is expressed as equations (5a) for digital CDS case and (5b) for analog CDS only case, respectively.

$$f_{SP} \approx 1/(T_2 - T_1) \text{ for digital CDS} \quad (5a)$$

$$f_{SP} \approx 1/(T_2 - T_0) \text{ for analog CDS only} \quad (5b)$$

Fig. 4 shows conceptual noise PSD change in DPS. Pixel comparator bias current needs to be small in DPS to limit the total surge current. It leads to increased e_n and reduced f_{CO} (nBW). Additionally, the limited comparator size makes FN large because it is inversely proportional to $\sqrt{LW}$ of MOS transistor gate area. As a result, PSD changes from the dark gray region to the light gray region as shown in Fig. 4, and FN becomes dominant in small pixel DPS.

One RN suppression technique in column-parallel SS-ADC is as follows. Noise floor e_n can be reduced by increasing the bias current, and nBW can be lowered with a larger C_{bw} to make TN small at the expense of power consumption. Some pixel-parallel SS-ADC demonstrated low noise with relatively large C_{bw} [5, 8], however it is only available with specific device processes.

C_{bw} effect is shown in Fig. 5 with the RN characteristics calculated in equation (4). A higher C_{bw} reduces RN effectively but has diminishing return once C_{bw} becomes relatively large. FN becomes the major contributor to RN in DPS with a relatively small C_{bw}. RN at T0 shown in Fig. 3 (a) becomes similar to RN at T1 when FN becomes the main contributor, suggesting regressed D-CDS effect on RN suppression. In addition, actual RN at T1 becomes larger in transient noise characteristics compared to AC noise calculation, and it depends on ramp slope [10]. We need to consider RN by transient analysis.

FN component in equation (4) can be expressed as equation (6). Flicker noise coefficient K and unit capacitance of MOS transistor C_{ox} depends on available device.

$$v_{ni\_FN}{}^2 = \frac{K}{C_{ox}WL}\left(ln\frac{f_{CO}}{f_{SP}} + b\right) \quad (6)$$

Fig. 6 shows FN PSD modulated by CDS operation. Both log and linear scale plots are presented. The frequency in X axis is normalized by f_{SP}. f_{SP} by itself does not impact FN after CDS, because integral PSD multiplied by the CDS transfer function from DC to f_{SP} yields constant value (expressed by "b" in this case). For example, $f'_{SP} = f_{SP}/n$ is applied, PSD in f'_{SP} case is n times larger than that in f_{SP} case, resulting a constant integral value. Ratio of f_{CO} and f_{SP} determines FN voltage as shown in equation (6) but lowering f_{CO} (nBW) does not efficiently work because noise PSD becomes small in the high frequency region as shown in Fig. 6.

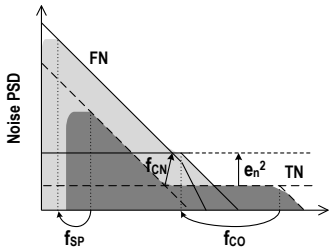

Fig. 4 Conceptual noise PSD change from column-parallel ADC (Dark gray) to pixel-parallel ADC (Light gray)

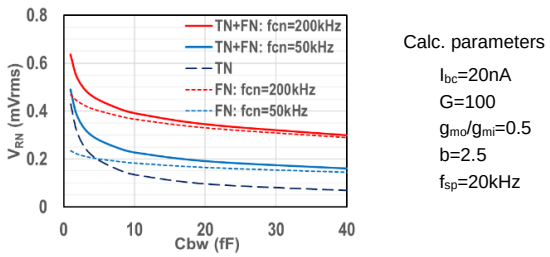

Fig. 5 Cbw effect for TN and FN.

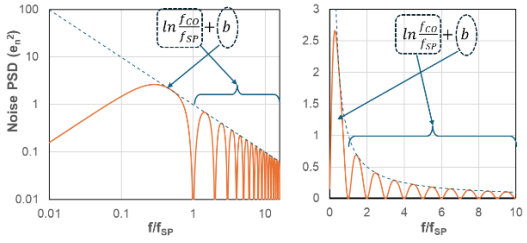

Fig. 6 FN PSD after CDS modulation

IV. High gain single-ended comparator

Instead of large C_{bw}, large open-loop gain helps reduce TN at T2 in Fig. 2 according to equation (4). RN can be suppressed by increasing C_C even with a small C_{bw} at T0. Comparable RN to D-CDS is available in this design strategy with a single memory bank for a small pixel size DPS.

Single-ended amplifier instead of differential amplifier in Fig. 1 also helps pixel size reduction. Fig. 7 shows the pixel configuration using single-ended comparator [11] for 3.24um DPS pixel. Active pixel has LOFIC structure to achieve high DR with multiple quantization operation in single exposure [6, 7, 11]. Ramp signal for SS-ADC is given through additional input capacitor C_R. This comparator structure has 2 advantages compared to differential amplifier. The first is design flexibility in small pixel size. Simple configuration enables relatively large transistor size for smaller FN and large gain. Second is larger ADC range under lower supply voltage, which is due to the comparator flipping at the same input voltage regardless of pixel signal voltage V_{SF}.

Although single-ended comparator has a disadvantage that signal is attenuated by a ratio of $C_C/(C_C + C_R)$ at V_{in}, it is not critical on the viewpoint of S/N ratio. It is because RN of ${v_{ni}}^2$ in equation (4) becomes 1/2 when single-ended amplifier is applied as comparator input stage. It means RN of v_{ni} becomes $1/\sqrt{2}$ times of that in differential amplifier. If $C_C/(C_C + C_R) = 2/3$, small RN of a single-ended comparator can almost compensate signal reduction and achieve almost same S/N ratio.

We evaluated 2 types of inverters. One applies cascode configuration of pMOS load transistor as shown in Fig. 7. Their gates are connected to bias voltage V_{bp0} and V_{bp1}, respectively. Open-loop gain of this configuration is around 200. The other applies simplified inverter, where cascode pMOS of V_{bp1} is removed. Open-loop gain is around 80.

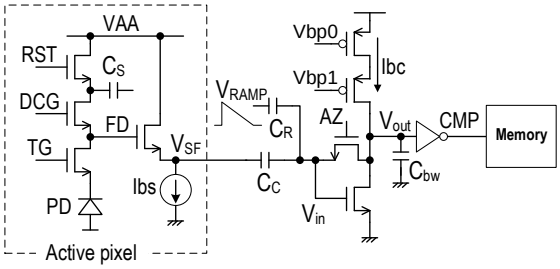

Fig. 7 Pixel configuration using single-ended comparator.

The design parameters and RN evaluation results of the test chips are summarized in Table 2. RN voltage at the source follower output (V_{SF}) is also compared in Fig.8. Lower noise voltage than the previous chip is achieved with smaller C_{bw}. Its contributors are large C_C and large open-loop gain G of single-ended amplifier.

Bias current dependency of RN in the test chips of 2 types of inverters, w/ cascode and w/o cascode, are shown in Fig. 9. Larger gain of the cascode circuit leads to smaller RN, and RN increases with a higher bias current. This trend is different from that in previous work in [7]. It had almost no dependency on bias current. This trend difference is caused by TN and FN ratio. If TN is the main factor in RN, no bias current dependency will be observed as shown in the first term in equation (4). On the other hand, the measurement results in Fig. 9 shows larger RN with higher bias current. It implies FN has a significant impact in these circuits under condition of $f_{CO} < f_{CN}$.

Small bias current decrease f_{CO} in equation (6) without FN PSD change, therefore RN becomes smaller with lower bias current. However, side effect might appear if f_{CO} becomes too low. RN is almost minimized at $I_{bc} = 20nA$ with the lowest RN of $v_{ni} = 0.4mVrms$ in this pixel size. Lower FN MOS device is desired for better RN performance in small pixel size DPS.

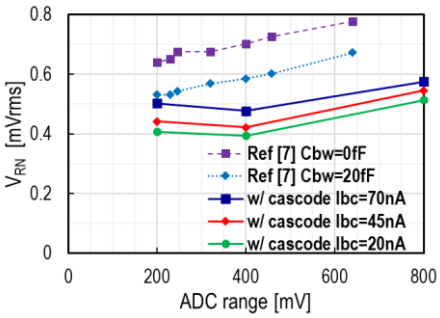

Fig. 8 RN performance comparison between reported DPS [7] and test chip.

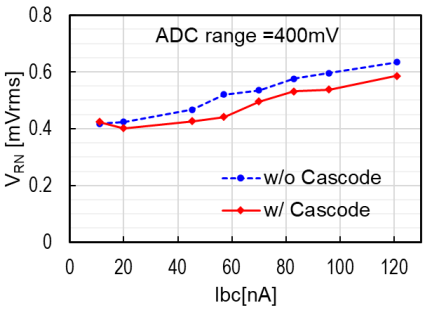

Fig. 9 Bias current dependency of RN performance in 2 types of inverter configuration.

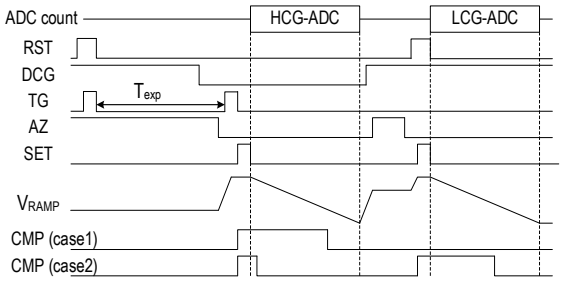

Fig. 10 Timing diagram of single exposure dual SS-ADC combining HCG and LCG

To achieve small RN in equivalent electron number, we designed this pixel to have high conversion gain (HCG) of 200uV/e- in this pixel. Thanks to this HCG, the test chip demonstrated 2.4e-rms RN with an ADC range of 400mV.

One drawback of HCG is small full-well capacity (FWC). To overcome this issue, a dual SS-ADC quantization operation with HCG and low conversion gain (LCG) is proposed in this

work. While a triple quantization operation is reported [6, 7, 11], which combined HCG, LCG and a nonlinear time-to-saturation scheme, this dual SS-ADC quantization scheme offers higher linearity, which is more suitable for color image capture.

Fig. 10 shows dual SS-ADC operation in single-exposure. LCG SS-ADC is conducted with DCG=H connecting C_S to FD after HCG SS-ADC. There is in-pixel control circuit to control whether overwrite the HCG data on memory by the LCG data (case 2) or not (case 1). In this control scheme, pixel memory is only 10 bits for 9-bit HCG ADC and 9-bit LCG ADC. Ratio of HCG and LCG is set smaller at around 10, which is smaller than that of the previous work of [7] for smaller SNR drop at junction point between HCG and LCG, which is measured at 28 dB. The dual quantization operation achieved high DR of 78dB.

V. Conclusion

RN in small pixel DPS is discussed. FN easily becomes the main contributor to RN with relatively small C_{bw} with bias current and area restriction. Digital CDS is not an efficient solution for RN reduction in small-pixel DPS with the doubled in-pixel memory area requirement. A solution with a single-ended comparator with high gain is proposed to reduce RN of DPS. We developed a DPS with 3.24 um pixel and confirmed the RN reduction. HCG of 208uV/e- achieved 2.4e-rms RN without D-CDS, and dual SS-ADC scheme with LCG enabled high DR of 78dB.

Table. 1 Symbol definition in equations.

Symbol	Definition	Symbol	Definition
e_n	Noise PSD of thermal noise	k	Boltzmann constant
G	Open-loop gain of 1st stage amp in comparator	T	Temperature
g_{mi} , g_{mo}	Transconductance of input/load MOS transistor	γ	Body-effect parameter
f_{CN}	Corner frequency (TN PSD=FN PSD)	C_{ox}	Unit capacitance of MOS transistor
f_{CO}	Cut off frequency	W, L	Width and Length of MOS transistor
f_{0dB}	Unity gain frequency	K	Flicker noise coefficient
f_{sp}	Sampling frequency in CDS operation.	v_{ni} , v_{no}	RN voltage at input, output
b	Flicker noise constant under f_{sp} in CDS.	v_{ni_FN}	FN voltage at comparator input.

Table. 2 Performance comparison with the previous chip.

Specification	Test chip	TED 2022 [7]
Process technology	45nm/40nm/40nm	45nm/65nm
Pixel size [μm]	3.24	4.6
Conversion Gain [μV/e-]	208/19.4	170/7
Comparator type	Single-ended input	Differential input
C_C [fF]	120	65
C_R [fF]	60	-
Cbw [fF]	5	20
Random noise [e-]	2.4	4.2

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